

**Amendments to the Claims:**

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**Claim 1 (Currently Amended):**

1. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

a' forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.

**Claim 2 (original):**

2. The method of claim 1, wherein said step of forming a metal drain plug further comprises self-aligning said metal drain plug to a respective drain electrode.

**Claim 3 (Currently Amended):**

3. A method for forming a flash memory device on a semiconductor assembly comprising forming a metal interconnect running a major length of a series of source electrodes

connected together by a conductively doped active area, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said metal interconnect having a majority of a bottom surface making contact to said conductively doped active area and spanning completely between neighboring gate electrodes.

**Claim 4 (Currently Amended):**

4. A method for forming a flash memory device on a semiconductor assembly comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a metal interconnect into said interconnect via, said metal interconnect running a major length of said connected together source electrodes and making contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line.

**Claim 5 (Currently Amended):**

5. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.

**Claim 6 (original):**

6. The method of claim 5, wherein said step of forming a metal drain plug further comprises self-aligning said metal drain plug to a respective drain electrode.

**Claim 7 (original):**

7. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a tungsten-based interconnect running a major length of said connected together source electrodes, said tungsten-based interconnect making a substantially continuous contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug connecting between a drain electrode of each said floating gate device and a digit line.

**Claim 8 (original):**

8. The method of claim 7, wherein said step of forming a tungsten-based drain plug further comprises self-aligning said tungsten drain plug to a respective drain electrode.

**Claim 9 (original):**

9. A method for forming a flash memory device on a semiconductor assembly comprising forming a tungsten-based interconnect running a major length of a series of source electrodes connected together by a conductively doped active area, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said tungsten-based interconnect having a majority of a bottom surface making contact to said conductively doped active area.

**Claim 10 (original):**

10. A method for forming a flash memory device on a semiconductor assembly comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a tungsten-based interconnect into said interconnect via, said tungsten-based interconnect running a major length of said source electrodes and making contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line.

**Claims 11-19 (withdrawn).**

**Claim 20 (new).**

20. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect consisting of a metal nitride barrier layer and an overlying metal layer, said metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.